48. (Third Amended) A capacitor comprising:

D2

a material layer having a first level and a second level, said first and second levels being connected by a sidewall region between said first and second levels;

Sub 7 E2

a post deposition doped BST high dielectric constant thin film material formed on at least one said sidewall region, wherein the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region; and

a capping layer provided over at least a portion of said BST thin film material.

74. (Third Amended) An integrated circuit capacitor device comprising:

D3

a material layer having a first level and a second level, wherein said first and second levels are connected by a sidewall region between said first and second levels;

Sub 7 E3

a first electrode provided at least on said sidewall region;

a post deposition doped BST high dielectric constant thin film material provided on at least one said first electrode, wherein the stoichiometry of said BST high dielectric thin film material is substantially uniform at least at said sidewall region; and

a second electrode provided on said BST high dielectric thin film layer.